REMARKS

In the Office Action, Claims 1-28 were examined and are rejected. In response to the Office Action, no claims are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-28 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. §103(a)

The Examiner has rejected Claims 1-4, 6-9, 11-13, 18-22 and 27-28 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No 4,949,280 to Littlefield ("Littlefield") in view of U.S. Patent No. 6,891,893 to Sullivan et al. ("Sullivan".) Applicants respectfully traverse this rejection.

Regarding Claim 1, Claim 1 recites the following claim features, which are neither taught nor suggested by the prior art combination of Littlefield in view of Sullivan:

> enabling a hardware accelerator selected from a plurality of hardware accelerators according to at least one bit of a register within the register file set by a processing element; and
> granting the processing element ownership over the selected hardware accelerator. (Emphasis added.)

In contrast to the above recited features of Claim 1, Littlefield discloses a parallel processor based raster graphic system architecture. As disclosed by Littlefield, the processing of graphic commands, the transferring of pixel data into a frame buffer, the rate at which the frame buffer can transfer pixel data to the display device as well as communications between units of a host computer and a graphic system can each create a potential bottleneck in generating raster images. (See col. 1, lines 34-43.)

To provide a system architecture referred to by Littlefield, (Col. 3, lines 41-48), Littlefield discloses an interconnection network. The interconnection network referred to by Littlefield (col. 4, lines 21-28) is illustrated with reference to Fig 3.

Although Littlefield discloses that second interconnection network 18 may be used to connect each processor 29 within host 28 with any of the graphic processor 12, as taught by Littlefield, in the simplest case, such interface can be eliminated and each application processor 29 within the host 28 is paired with a graphics processor 12. (Col. 7, lines 19-28.) We submit that application processors 29 of host application 28, as shown in FIG. 5, do not set a bit of a register in order to receive ownership of a specific one of the graphic processors (GP) 12, as in Claim 1. Furthermore, as disclosed by Littlefield, in the embodiment shown in FIG. 4, the graphics processors are assigned according to a first free basis.

In view of the above, assuming each application processes 29 of host 28 can connect with any graphics processors 12 shown in FIG. 5, Littlefield fails to teach how an application processor 29 select the respective graphics processor GP 12, as in Claim 1. Hence, the capability disclosed by Littlefield to enable connection between any AP 29 and any GP 12 via interconnection network 18 neither discloses, teaches or suggests enabling a hardware accelerator from a plurality of hardware accelerators according to at least one bit of register within the register file set by a processing element, as in Claim 1. As a result, the Examiner cites Sullivan.

Sullivan is generally directed to video processing and provides a multimedia application program interface (API) that automatically identifies and dynamically adapts to processing system capabilities to improve multimedia processing performance. In contrast with Claim 1, Sullivan fails to rectify the deficiencies of Littlefield to teach or suggest enabling a hardware accelerator selected from a plurality of hardware accelerators according to at least one bit of a register, much less that the at least one bit of the register within a register file is set by a processing element, as in Claim 1. Sullivan does disclose an auto-negotiation data structure 202 that is selectively invoked by a media processing system element to identify the media processing capabilities of the media processing system (see, Col. 8, lines 27-30), however, that is something completely different from enabling a hardware accelerator selected from a plurality of hardware accelerators according to at least one bit of a register within the register file set by a processing element, as in Claim 1.

Sullivan discloses API 104 which identifies the operational capabilities of the multimedia processing system elements and selectively negotiates the processing of received multimedia content among these elements to improve multimedia processing performance. (See, Col. 8, lines 8-14.) Hence, API 104 facilitates the interoperability of any decoder application (160(A) – 160(N)) with any multimedia accelerator (174(A) – 174(N)) (see, Col. 8, lines 15-17), however, that is something completely different from the enabling of a hardware accelerator according to a bit set by a processing element to select the hardware accelerator as in Claim 1.

In contrast with Claim 1, the process of finding a multimedia accelerator 174 that agrees to a decoding acceleration capability that is acceptable to both the decoder and the accelerator (see Sullivan, Col. 27, lines 39-42) does not teach or suggest enabling a hardware accelerator according to a bit within a register file that is set by a processing element to select a hardware accelerator much less the granting of a processing element ownership over the selected hardware accelerator, as in Claim 1. In contrast with the selection of a hardware accelerator by a processing element, Sullivan teaches that the media processing element (e.g., decoder 160) iteratively issues configuration commands until a response is received from one of the multimedia accelerators (174(A) – 174(N)) to an issued auto-negotiation data structure 202 to indicate that the multimedia accelerator supports the media processing format defined in the auto-negotiation data structure 202. (See, col. 27, lines 39-42 and lines 51-56.)

Hence, we submit that the disclosure of Sullivan is limited to acceptance, by a multimedia accelerator 174, of a proposed media processing format defined in an auto-negotiation data structure issued by a decoder application 160. (See, supra.) Hence, we submit that the decoder 160 (processing element), as disclosed by Sullivan, does not set at least one bit of a register within a register file to select a multimedia accelerator (processing element), as in Claim 1.

Apposite to Claim 1, Sullivan teaches that the processing element (e.g., decoder 160) repeatedly issues requests until a multimedia accelerator 174 issues a response that the accelerator 174 supports a proposed media processing format defined in an auto-negotiation data structure. In other words, assuming, arguendo, that the decoder application 160 desired

ownership over a hardware accelerator, such as an accelerator 174, a negative response to an auto-negotiation data structure, issued by decoder application 160, would prohibit such ownership, in contrast to Claim 1. Hence, we submit that the prior art combination of Littlefield in view of Sullivan fails to teach or suggest the enabling of a hardware accelerator according to at least one bit of a register file set by a processing element to select the hardware accelerator, as in Claim 1.

For each of the above reasons, therefore, Claim 1 and all claims which depend from Claim 1 are patentable over the prior art combination of Littlefield in view of Sullivan.

Each of Applicants' other independent claims includes limitations similar to those in Claim 1 discussed above. Therefore, all of Applicants' other independent claims, and all claims which depend on them, are also patentable over the cited art, for similar reasons.

DEPENDENT CLAIMS

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as an agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 3/21/07

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____ 3/21/07
Suzanne Johnston Date